REMARKS

Claims 1-12 are pending in the application.

Claim Rejections under 35 USC §102

Claims 1, 3 and 12 are rejected under 35 USC §102(e) as being anticipated by Arita et al. (U.S. Patent No. 6,046,490).

In rejecting the claimed invention, the outstanding Office Action has specifically stated that:

> "Arita shows (fig. 1) a semiconductor device comprising a transistor having a first and second impurity region (3) formed in a substrate (1), and a gate electrode (5). A first insulating layer (6) covers the transistor. A capacitor (10) is formed on the insulating layer, the capacitor having a dielectric (8) formed of a high dielectric constant material (col. 8, lines 39-45), and an upper electrode (9) and tower electrode (7) with the dielectric positioned therebetween. A silicon oxide film (22) is formed over the capacitor and has its upper surface planarized. A silicon nitride oxide film (14) is formed on the oxide to prevent moisture from penetrating the device (col. 6, lines 10-17). A second insulating film (15) is formed between the capacitor and the silicon oxide film.
>
> With respect to the limitation of the "nitrogen being introduced all over the planarized surface of the silicon oxide film, a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 **USPQ 15** at 17(footnote 3). See also in re Brown, 173 **USPQ** 685: In re Luck, 177 **USPQ** 523, In re Fessmann, **180 USPQ 324**; In re Avery, **186 USPQ 116** in re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al, 218 **USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above case law makes clear. "Even though product-by- process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does

> not depend on its method of production. It the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted)."

The Applicant respectfully disagrees with this Office position. In claim 1, nitrogen resides on top of the surface of the silicon oxide film. Consequently, it is able to keep moisture from entering into the silicon oxide film.

Regarding Arita, as explained in the outstanding Office Action, the silicon oxide (22) has been positively cited to be correspondent to a silicon oxide of the claimed invention. As clearly shown in Figure 1 of Arita, on the silicon oxide (22), a passivation layer (14) is formed.

Though the Examiner asserts that the upper surface of the oxide includes nitrogen because a passivation layer (14) is formed on the oxide, the claimed invention is not anticipated because, in Arita, nitrogen is not included in the upper surface of the oxide directly under wirings (19a), (19b) and the insulating layer (21). Therefore, the passivation layer 14 cannot protect moisture from coming into contact with either wirings (19a), (19b) or the insulating layer (21).

However, the present invention is able to prevent moisture from entering into the silicon oxide thereby preventing formation of any film on the silicon oxide, for instance, any silicon nitride film.

Even though the claim language is not a product by process claim, to further eliminate the possibility of mis-interpreting the claim language as a product by process claim, and to incorporate the comments of the Examiner made during a personal interview on October 10, 2002, independent

claims 1 and 12 have been further amended so that any reasonable interpretation thereof would properly regard each as a product claim. Independent claims 1 and 12, as amended, are reproduced hereinbelow for the convenience of the Office:

"1. (Twice Amended) A semiconductor device, comprising;

a contact;

a transistor having a first impurity region and a second impurity region formed on a semiconductor substrate, and a gate electrode formed on the semiconductor substrate;

a first insulating film [for covering] on top of the transistor;

a capacitor formed on the first insulating film, the capacitor having a dielectric film [formed] made of [either] one of a ferroelectric material [or] and a high-dielectric material, and an upper electrode and a lower electrode positioned to put the dielectric film therebetween; and

a silicon oxide film [placed over] residing on top of the capacitor [forming] to form a planarized surface;

wherein nitrogen [being introduced all] resides over the planarized surface of the silicon oxide film; and

wherein the contact is positioned above the silicon nitride film including nitrogen."

"12. (Twice Amended) a semiconductor device, comprising:

a contact;

a transistor having a first impurity region and a second impurity region formed on a semiconductor substrate, and a gate electrode formed on the semiconductor substrate;

a first insulating film [for covering] on top of the transistor;

a capacitor formed on the first insulating film, the capacitor having a dielectric film [formed of either] made of one of a ferroelectric material [or] and a high-dielectric material, and an upper electrode and a lower electrode positioned to put the dielectric film therebetween;

a second insulating film [covering] on top of the capacitor to [become] serve as an upper planarized surface; [and]

wherein [a surface of the second insulating film is planarized and] nitrogen [is introduced by plasma processing all over] resides on top of the upper planarized surface of the second insulating film; and

wherein the contact is positioned above the silicon nitride film including nitrogen."

As it is now clear that nitrogen reside over the planarized surface, any reasonable interpretation of this claim should focus upon the presence of elements rather than any process related thereto.

It is well settled that:

> "A claim is anticipated only if each and every element *as set forth in the claim* is found, either expressly or inherently described, in a single prior art reference." *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1567, 7 USPQ2d 1057 (Fed. Cir. 1988)."

Should the Office believe that independent claims 1 and 12, as amended, are anticipated by Arita, a citation of where each and every element of the claimed invention is disclosed in Arita is respectfully requested.

It is respectfully submitted that independent claims 1 and 12, as amended, patentably distinguish over Arita. All claims dependent thereon, by virtue of inherency, also patentably distinguish over Arita. Reconsideration and withdrawal of this rejection are respectfully requested.

As an effort to assist the Office to determine whether indeed each and every element of the claimed invention is disclosed in the prior art, the following claims with parenthetical blanks are submitted herewith.

1. (Twice Amended) A semiconductor device ( ), comprising;

a contact ( );

a transistor ( ) having a first impurity region ( ) and a second impurity region ( ) formed on a semiconductor substrate ( ), and a

gate electrode ( ) formed on the semiconductor substrate ( );

a first insulating film ( ) on top of the transistor ( );

a capacitor ( ) formed on the first insulating film ( ), the capacitor having a dielectric film ( ) made of one of a ferroelectric material ( ) and a high-dielectric material ( ), and an upper electrode ( ) and a lower electrode ( ) positioned to put the dielectric film therebetween ( ); and

a silicon oxide film ( ) residing on top of the capacitor ( ) to form a planarized surface ( );

wherein nitrogen ( ) resides over the planarized surface ( ) of the silicon oxide film ( ); and

wherein the contact ( ) is positioned above the silicon nitride film ( ) including nitrogen ( ).

12. (Twice Amended) a semiconductor device ( ), comprising:

a contact ( );

a transistor ( ) having a first impurity region ( ) and a second impurity region ( ) formed on a semiconductor substrate ( ), and a gate electrode ( ) formed on the semiconductor substrate ( );

a first insulating film ( ) on top of the transistor ( );

a capacitor ( ) formed on the first insulating film ( ), the

capacitor ( ) having a dielectric film ( ) made of one of a ferroelectric material ( ) and a high-dielectric material ( ), and an upper electrode ( ) and a lower electrode ( ) positioned to put the dielectric film therebetween ( );

a second insulating film ( ) on top of the capacitor ( ) to serve as an upper planarized surface ( );

wherein nitrogen ( ) resides on top of the upper planarized surface ( ) of the second insulating film ( ); and

wherein the contact ( ) is positioned above the silicon nitride film ( ) including nitrogen ( ).

Claim Rejections under 35 USC §103

Claims 2 and 4 are rejected under 35 USC §103(a) as being unpatentable over Arita et al. (U.S. Patent No. 6,046,490) in view of Singh et al. (U.S. Patent No. 5,847,464).

As independent claim 1 has been patentably distinguished over Arita, all claims dependent thereon, including claims 2 and 4, by virtue of inherency, also patentably distinguished over Arita further in view of whatever secondary reference.

Reconsideration and withdrawal of this rejection are respectfully requested.

Claims 5 and 9-11 are rejected under 35 USC §103(a) as being unpatentable over Mochizuki et al. (U.S. Patent No. 5,990,507) in view of Arita et al. (U.S. Patent No. 6,046,490).

In rejecting the claimed invention, the outstanding Office Action has specifically stated that:

"Mochizuki et al. shows (fig. 17) a semiconductor device comprising a transistor having a first and second impurity region (S, D) formed in a substrate (1), and a gate electrode (G, 4 & 5). A first insulating layer (10) covers the transistor. A capacitor is formed on the insulating layer, the capacitor having a dielectric (18) formed of a ferroelectric material, and an upper electrode (19) and lower electrode (17) with the dielectric positioned therebetween. A second insulating film (13) is formed on the capacitor. A local interconnection (22) is formed on the second insulating film for connecting the upper electrode of the capacitor to the first impurity region (S). Third insulating film (30) is formed on the local interconnection and the second insulating film. A first wiring (BL) is formed on the third insulating film and electrically connects to the second impurity region (D)via a hole which is formed in the first, second, and third insulating films. A fourth insulating film (39) is formed on the first wiring and has a planarized upper surface. The upper surface of the first insulating film is planarized. A second wiring is formed on the fourth film and connects to the first wiring via a hole formed through the fourth insulating layer (col. 24, lines 49-67). Mochizuki shows all of the elements of the claims except the third and fourth insulating films formed specifically of silicon oxide. Arita shows (fig. 1) a semiconductor device comprising a transistor having a capacitor device covered by third and fourth insulating films, which are formed of silicon oxide (col. 6, lines 1-17). A silicon nitride oxide film (14) is formed on the oxide. With this configuration, moisture is prevented from penetrating the device (col. 6, lines 10-17). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the insulating layers Mochizuki by forming oxide and then oxynitride as taught by Arita to prevent moisture from penetrating the device.

With respect to the limitation of the "nitrogen being introduced all over the planarized surface of the silicon oxide film,' a "product by process claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17**(footnote 3). See also in re Brown, **173 USPQ 685**; In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**; In re Avery, **186 USPQ 116** ; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al, **218 USPQ 289** final product per se which must be determined in a product by, all of claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above case law makes clear. Even though

> product-by-process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985)(citation. omitted)."

The Applicant respectfully disagrees with the Office position. In claim 5, nitrogen resides on top of the surface of the silicon oxide film. Consequently, it is able to keep moisture from entering into the silicon oxide film.

Regarding Mochizuki, as explained in the outstanding Office Action, a second layer flattening interlayer insulation film (13) has been positively cited to be correspondent to a silicon oxide film of the claimed invention. As clearly shown in Figure 17 of Mochizuki, on the first interlayer insulation film (10), the second layer flattening interlayer insulation film (13) is formed.

Though the Examiner may have regarded that the first interlayer insulation film (10) includes nitrogen because the second layer flattening interlayer insulation film (13) formed thereon, the claimed invention is not anticipated because in Mochizuki, nitrogen is not included in the first interlayer insulation film (10) directly under contact plugs (33), (34). Therefore, the second layer flattening interlayer insulation film (13) cannot protect moisture from coming into contact plugs (33), (34).

However, the present invention is able to prevent moisture from entering into the silicon oxide thereby preventing formation of any film on the silicon oxide, for instance, any silicon nitride film.

Even though the claim language is not a product by process claim, to further eliminate the

possibility of mis-interpreting the claim language as a product by process claim, and to incorporate the comments of the Examiner made during a personal interview on October 10, 2002, independent claim 5 has been further amended so that any reasonable interpretation thereof would properly regard it as a product claim. Independent claim 5, as amended, is reproduced hereinbelow for the convenience of the Office:

" 5. (Twice Amended) A semiconductor device, comprising[;]:
a contact;
a transistor having a first impurity region and a second impurity region formed on a semiconductor substrate, and a gate electrode formed on the semiconductor substrate;
a first insulating film [for covering] residing on top of the transistor;
a capacitor formed on the first insulating film, the capacitor having a dielectric [formed] made of [either] one of ferroelectric material [or] and a high-dielectric material, and an upper electrode and a lower electrode positioned to put the dielectric film therebetween;
a second insulating film formed on the capacitor;
a local interconnection formed on the second insulating film[, for] to electrically connecting the upper electrode of the capacitor [to] with the first impurity region;
a third insulating film formed on the local interconnection and the second insulating film;
a first wiring formed on the third insulating film and electrically connected to the second impurity region via a hole which is formed on the first insulating film, the second insulating film, and the third insulating film;
a fourth insulating film [placed] on top of the first wiring [forming] to serve an upper planarized surface,
wherein nitrogen [being introduced all over] resides on top of the upper planarized surface of the fourth insulating film; [and]
wherein the contact is positioned above the silicon nitride film including nitrogen; and
a second wiring formed on the fourth insulating film."

As it is now clear that nitrogen reside over the upper planarized surface, any reasonable interpretation of this claim should focus upon the presence of elements rather than any process related thereto.

Section 2143 of the MPEP has specifically stated that:

> "To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference must teach or suggest all the claimed limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 466, 20 USPQ2d 1438 (Fed. Cir. 1991)."

Therefore, it is both a court position and a Patent Office position that to establish a *prima facie* case of obviousness, 1) there **must be** some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings; 2) there **must be** a reasonable expectation of success; and 3) the teaching or suggestion to make the claimed combination and the reasonable expectation of success **must both be** found in the prior art, and not based on applicant's disclosure.

Should the Office finds that none of the prior art references is either unable to identified each and every aspect of the above-mentioned claimed features therein, or the formulated rejection simply would not arise to a level objectively fulfilling all three criteria of establishing a *prima facie* case of obviousness, it is respectfully submitted that the obviousness rejection would be defective and allowance of the claimed invention is requested.

As an effort to assist the Office to determine whether indeed each and every element of the claimed invention is disclosed in the prior art, the following claims with parenthetical blanks are submitted herewith.

5. (Twice Amended) A semiconductor device ( ), comprising[;]:

a contact ( );

a transistor ( ) having a first impurity region ( ) and a second impurity region ( ) formed on a semiconductor substrate ( ), and a gate electrode ( ) formed on the semiconductor substrate ( );

a first insulating film ( ) residing on top of the transistor ( );

a capacitor ( ) formed on the first insulating film ( ), the capacitor having a dielectric ( ) made of one of ferroelectric material ( ) and a high-dielectric material ( ), and an upper electrode ( ) and a lower electrode ( ) positioned to put the dielectric film therebetween ( );

a second insulating film ( ) formed on the capacitor ( );

a local interconnection ( ) formed on the second insulating film ( ) to electrically connecting the upper electrode ( ) of the capacitor ( ) with the first impurity region ( );

a third insulating film ( ) formed on the local interconnection ( ) and the second insulating film ( );

a first wiring ( ) formed on the third insulating film ( ) and electrically connected to the second impurity region ( ) via a hole ( ) which is formed on the first insulating film ( ), the second insulating film ( ), and the third insulating film ( );

a fourth insulating film ( ) on top of the first wiring ( ) to serve

an upper planarized surface ( ),

wherein nitrogen ( ) resides on top of the upper planarized surface ( ) of the fourth insulating film ( );

wherein the contact ( ) is positioned above the silicon nitride film ( ) including nitrogen ( ); and

a second wiring ( ) formed on the fourth insulating film ( ).

Claims 6-8 are rejected under 35 USC §103(a) as being unpatentable over Mochizuki et al. (U.S. Patent No. 5,990,507) in view of Arita et al. (U.S. Patent No. 6,046,490) and further in view of Singh et al. (U.S. Patent No. 5,847,464).

As independent claim 5 has been patentably distinguished over Mochizuki in view of Arita, all claims dependent thereon, including claims 6-8, by virtue of inherency, also patentably distinguished over Mochizuki in view of Arita further in view of whatever other secondary reference.

Reconsideration and withdrawal of this rejection are respectfully requested.

Prior Art Indicated To Be Pertinent To The Disclosure

The Office has provided a list of prior art indicated to be pertinent to the Applicant's invention. Consistent with the understanding as stipulated in MPEP 706.02 that only the best prior art should be applied, this list of prior art not having been applied by the Office, it is the Applicant's understanding that the Office must have considered the listed prior art to be no more pertinent than the applied prior art of record.

Conclusion

In view of the aforementioned amendments and accompanying remarks, claims 1, 5 and 12, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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Enclosures: Version with markings to show changes made
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VERSION WITH MARKINGS TO SHOW CHANGES MADE 09/594,091

IN THE TITLE:

SEMICONDUCTOR MEMORY DEVICE [AND METHOD OF MANUFACTURING THE SAME] HAVING PLANARIZED UPPER SURFACE AND A SiON BARRIER

IN THE CLAIMS:

Please amend claims 1, 5 and 12 as indicated below:

1. (Twice Amended) A semiconductor device, comprising[;]:

a contact;

a transistor having a first impurity region and a second impurity region formed on a semiconductor substrate, and a gate electrode formed on the semiconductor substrate;

a first insulating film [for covering] on top of the transistor;

a capacitor formed on the first insulating film, the capacitor having a dielectric film [formed] made of [either] one of a ferroelectric material [or] and a high-dielectric material, and an upper electrode and a lower electrode positioned to put the dielectric film therebetween; and

a silicon oxide film [placed over] residing on top of the capacitor [forming] to form a planarized surface;

wherein nitrogen [being introduced all] resides over the planarized surface of the silicon oxide film; and

wherein the contact is positioned above the silicon nitride film including nitrogen.

5. (Twice Amended) A semiconductor device, comprising[;]:

a contact;

a transistor having a first impurity region and a second impurity region formed on a semiconductor substrate, and a gate electrode formed on the semiconductor substrate;

a first insulating film [for covering] residing on top of the transistor;

a capacitor formed on the first insulating film, the capacitor having a dielectric [formed] made of [either] one of ferroelectric material [or] and a high-dielectric material, and an upper electrode and a lower electrode positioned to put the dielectric film therebetween;

a second insulating film formed on the capacitor;

a local interconnection formed on the second insulating film[, for] to electrically connecting the upper electrode of the capacitor [to] with the first impurity region;

a third insulating film formed on the local interconnection and the second insulating film;

a first wiring formed on the third insulating film and electrically connected to the second impurity region via a hole which is formed on the first insulating film, the second insulating film, and the third insulating film;

a fourth insulating film [placed] on top of the first wiring [forming] to serve an upper planarized surface,

wherein nitrogen [being introduced all over] resides on top of the upper planarized surface of the fourth insulating film; [and]

wherein the contact is positioned above the silicon nitride film including nitrogen; and

a second wiring formed on the fourth insulating film.

12. (Twice Amended) a semiconductor device, comprising:

a contact;

a transistor having a first impurity region and a second impurity region formed on a semiconductor substrate, and a gate electrode formed on the semiconductor substrate;

a first insulating film [for covering] on top of the transistor;

a capacitor formed on the first insulating film, the capacitor having a dielectric film [formed of either] made of one of a ferroelectric material [or] and a high-dielectric material, and an upper electrode and a lower electrode positioned to put the dielectric film therebetween;

a second insulating film [covering] on top of the capacitor to [become] serve as an upper planarized surface; [and]

wherein [a surface of the second insulating film is planarized and] nitrogen [is introduced by plasma processing all over] resides on top of the upper planarized surface of the second insulating film; and

wherein the contact is positioned above the silicon nitride film including nitrogen.